20 YEARS of
ALTERA®
INNOVATION

SOPC
arkkitehtuurit
ja suunnittelu

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Highlights

- Founded in 1983
- $839 Million in 2001 Sales
- 1,875 Employees
- 14,000+ Customers Worldwide
The Programmable Solutions Company

High-Density CMOS Programmable Logic Devices

Intellectual Property

Development Software
Altera Product Positioning

CPLDs

Low Cost

General Purpose

FPGAs with Embedded Transceivers

FPGAs with Embedded Processors
All New Product Portfolio (0.13-um)

- Highest Density FPGA in Production Today
- Up to 10 Mbits of TriMatrix™ Memory
- DSP: High-Speed Digital Signal Processing Blocks
- PLL: Advanced Clock Management Circuitry
- DDR: External Memory Interface Circuitry

- Industry’s Lowest Cost FPGA Family
- Designed for Low Cost from the Ground Up
- 4X the Density of Previous Low-Cost Architectures
- Designed Based on Customer Requirements

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## All-Layer Copper Experience

<table>
<thead>
<tr>
<th>0.15-um Copper</th>
<th>Status</th>
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<tbody>
<tr>
<td>EP20K200C</td>
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<tr>
<td>EP20K400C</td>
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<tr>
<td>EP20K600C</td>
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<tr>
<td>EP20K100C</td>
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<tr>
<td>EP2A25</td>
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<tr>
<td>EP2A40</td>
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<tr>
<td>EP1M120</td>
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<tr>
<td>EP1M350</td>
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<td><strong>Total</strong></td>
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- ✔ Engineering Sample Availability
- ✔ Production Availability

<table>
<thead>
<tr>
<th>0.13-um Copper</th>
<th>Status</th>
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<tbody>
<tr>
<td>EP2A70</td>
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<td>EP1S10</td>
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<td>EP1S20</td>
<td>✔</td>
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<td>EP1C20</td>
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<td>EP1C12</td>
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<td>EP1SGX25</td>
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<td><strong>Total</strong></td>
<td><strong>9</strong></td>
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Fixed Costs for SoC / ASIC

- NRE Cost
  - $500K+

- Fab Write Off
  - $2Bn+ over 3 years
Wafer Foundry Example

ASIC Model

- Unique mask set needed per customer per design
- High mask charges
- High minimum order quantities

PLD Model

- One mask set serves 1,000s of customers in 1,000s of applications
- No separate mask charges (NRE)
- No minimum order quantity
Managing Time-to-Market Is Critical

2-Year Product Life Cycle

Volume

Time

Price
Managing Time-to-Market Is Critical

Two year life-cycle products lose 34% of potential revenue and 50% of profit if they are 3 months late.

Source: McKinsey
Design Flows Are Simple Now…
System Construction
Terms

PLD = Programmable Logic Device
CPLD = Complex Programmable Logic Device
FPGA = Field Programmable Gate Array
SOPC = System On Programmable Chip
LE = Logic Element
LUT = Look-Up Table
Hard Core = Embedded CPU on silicon
Soft Core = Embedded CPU implemented with FPGA.
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SOPC solutions
Complexity – Transistors over Time

1985: PLD transistor count one order of magnitude behind leading microprocessor

2002: PLD (EP1S80) ~5x transistor count of latest Pentium 4
Price Trend

Price per Logic Element (LE) Driven Lower Each Year

Price per LE Sold (Normalized to Q1 1993)
PLD Evolution

1996:
- 100k-gate 0.5µm EPF10K100 is the PLD state-of-the-art
- An 8-bit 8051 core fills it and runs at 5 MHz

$200 per processor MHz

2001:
- 1.5M-gate 0.18µm EP20K1500E in volume production
- A 32-bit Nios processor takes 2% of its capacity and runs at 50MHz

$0.33 per processor MHz
Excalibur Approach to SOPC

- RISC processors targeted for programmable logic
  - Hard & soft
- System configuration tools to automate SOPC design
- Standard, off-the-shelf devices
- Affordable & widely accessible
Embedded Processor Solutions

Embedded Processors Provide Flexibility & Horsepower for Broad Market Coverage

Performance (MIPS)

Soft Core

Hard Core

ARM® Core

Nios®
ARM-Based Excalibur Device

- ARM922T Stripe
  - Hard Logic
- 200 MHz
- 210 DMIPS
- Programmable Logic
  - 100K Gates to 1M Gates
- Three Devices in Family

All Available Today
# The Altera Excalibur Approach

## Industry’s First Embedded Processor PLD Solutions

<table>
<thead>
<tr>
<th>Processor Subsystem</th>
<th>Interfaces &amp; Debug Logic</th>
<th>EPXA1</th>
<th>EPXA4</th>
<th>EPXA10</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>32 Kbytes SRAM</td>
<td>128 Kbytes SRAM</td>
<td>256 Kbytes SRAM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16 Kbytes DPRAM</td>
<td>64 Kbytes DPRAM</td>
<td>128 Kbytes DPRAM</td>
</tr>
<tr>
<td>EPXA1</td>
<td></td>
<td>4,160 LEs (100,000 Gates)</td>
<td>53 Kbits RAM</td>
<td></td>
</tr>
<tr>
<td>EPXA4</td>
<td></td>
<td>16,640 LEs (400,000 Gates)</td>
<td>212 Kbits RAM</td>
<td></td>
</tr>
<tr>
<td>EPXA10</td>
<td></td>
<td>38,400 LEs (1,000,000 Gates)</td>
<td>327 Kbits RAM</td>
<td></td>
</tr>
</tbody>
</table>

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Excalibur ARM Configuration

SDRAM
Flash
ROM
SRAM

Watchdog Timer
Interrupt Controller
ARM922T Processor

ETM9

AHB 1-2 Bridge

Configuration Register

PLD-to-Stripe Bridge
Dual-Port SRAM
Single-Port SRAM

Phase-Locked Loop (PLL)
Reset Module
Timer

Expansion Bus Interface (EBI)

AHB1
AHB2

AHB

FPGA Logic

Programmable Logic Master Peripheral
Programmable Logic Module
Programmable Logic Module

Excalibur Hard Processor
IP
External Devices

Programmable Logic Slave Peripheral
Programmable Logic Slave Peripheral

AHB: AMBA™ High-Performance Bus
Excalibur Work Flow

Peripheral Pool

User Peripherals

Verilog / VHDL Files

Configure System

Generate

SOPC Builder

C Header Files

Peripheral Drivers

Quartus™ Software

User Design

Other IP

Hardware

User Code

Libraries

RTOS

Software

Native Core / Gnu Developer Suite

Executable

Debugger & Trace Analyzer

Excalibur Solution

Configuration

Trace

JTAG
EPXA1 Development Kit

- Excalibur EPXA1 development board
- Smart LCD module
- Power supply
- Connection cables
- SOPC Builder
- GNUPro Toolkit
- Documentation
- Quartus® II Web Edition design software
- Software, drivers, and application examples on CD-ROM
EPXA10 DDR Development Kit

- EPXA10 DDR development board
- Quartus® II Kit Edition (a time-limited version of the Quartus II software) with SOPC Builder and GNUPro Toolkit
- Software, drivers, and application examples on CD-ROM
- Power supply
- Connection cables
- Documentation
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SOPC
Excalibur Nios
Nios Embedded Processor

- Configurable Soft-Core Embedded Processor
- Optimized for Altera® FPGA Architecture
- 16-Bit Instruction Set RISC Architecture
  - 16- & 32-Bit Data Path
- License & Royalty Free
  - ASIC License Available
- Industry’s Most Popular Soft-Core Processor
Nios Processor Makes It onto Embedded Map in 2002
- Nios Is the Only Configurable CPU on the List

Planned Usage Grows 4x for 2003

Motorola 16-Bit Microcontrollers: Current Usage 28%, Planned Usage 23%
Embedded x86 (16 Bit): Current Usage 25%, Planned Usage 18%
Infineon (Siemens) C16x: Current Usage 8%, Planned Usage 9%
Microchip PIC: Current Usage 6%, Planned Usage 11%
Hitachi H8 Series: Current Usage 5%, Planned Usage 6%
ARM Thumb Family: Current Usage 4%, Planned Usage 4%
TI MSP 430: Current Usage 3%, Planned Usage 9%
Altera Nios (16 Bit*): Current Usage 1%, Planned Usage 4%
Nios Processor Block Diagram

- Standard RISC Components
- Optimized for Size & Performance in PLDs
- Fully Synchronous Interface

Instruction Fetch & Decode
Program Counter
Operand Fetch & Store
General-Purpose Register File
ALU
Interrupt Control

Instruction Address
Instruction in
16
Clock Enable
Clock
Wait
Reset

Read/Write
Byte Enable
Data Out
Data Address
Data In
IRQ
IRQL

IRQ: Interrupt Request
ALU: Arithmetic Logic Unit
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Custom Instruction

- Dramatic Boost in Processing Performance
  - No Increase in $f_{\text{MAX}}$
- Extends Nios Instruction Set
  - Up to Five Instructions
- SOPC Builder Development Tool
  - Automatically Adds User Logic to Nios ALU
  - Assigns Op-Code
  - Generates C & Assembly Macros
Nios Processor Systems

- Complete Microprocessor Subsystem
  - Processor Core
  - Memory Interfaces
  - Peripherals
  - Custom Logic
  - JTAG-Based On-Chip Debug Logic

- Avalon™ Switch Fabric
  - Connects All Components

- Multiprocessor Systems Possible

PIO: Parallel I/O
SPI: Serial Peripheral Interface

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Peripheral Components

- Memory Interface
  - On-Chip
    - RAM, ROM
  - Off-Chip
    - SDRAM Controller
    - SSRAM
    - SRAM
    - Flash, ROM
  - On-Chip Instruction & Data Cache

- DMA Controller
  - Memory-Peripheral
  - Memory-Memory
  - Peripheral-Peripheral

- Bridges
  - AHB to Avalon Bridge

- Parallel I/O (PIO) Registers
  - General-Purpose I/O Registers (PIO)
    - Input
    - Output
    - Bidirectional
  - User-Defined Interface

- Serial Interface
  - UART
  - SPI

- Timer
  - Simple Timer
  - Pulse Generator
  - Watchdog Timer

 INCLUDED IN NIOS DEVELOPMENT KIT!
# Design Example: Size & Speed

<table>
<thead>
<tr>
<th>Device Family</th>
<th>Standard 32-Bit Reference Design</th>
<th>Standard 16-Bit Reference Design</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>LEs</td>
<td>f&lt;sub&gt;MAX&lt;/sub&gt; (MHz)</td>
</tr>
<tr>
<td>Stratix</td>
<td>2,941</td>
<td>111</td>
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<tr>
<td>Cyclone</td>
<td>2,574</td>
<td>104</td>
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<tr>
<td>APEX II</td>
<td>3,046</td>
<td>55</td>
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<tr>
<td>APEX 20KC</td>
<td>3,022</td>
<td>53</td>
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<td>APEX 20KE</td>
<td>3,035</td>
<td>43</td>
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<tr>
<td>ACEX® 1K</td>
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SOPC Builder
SOPC Builder Flow

**Hardware Development**
- Processor Library
- Peripheral Library

**SOPC Builder GUI**
- Configure Processor
- Select & Configure Peripherals, IP
- Connect Blocks
- Generate

**Software Development**
- Custom Instructions
- IP Modules

**Synthesis & Fitter**
- EDIF Netlist
- HDL Source Files
- Testbench

**Verification & Debug**
- User Design
- Other IP Blocks

**On-Chip Debug**
- JTAG, Serial, or Ethernet

**C/C++ Compiler**
- User Code
- Libraries
- RTOS

**Quartus II**
- User Design
- Other IP Blocks

**Generate**
- EDIF Netlist
- HDL Source Files
- Testbench

**Executable Code**
- User Code
- Libraries
- RTOS

**Quartus II**
- User Design
- Other IP Blocks

**SignalTap II**
- Software Trace
- Hard Breakpoints
- SignalTap II

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Customization - Just What You Need

- Pool of “SOPC Builder Ready” Components
  - Communications
  - DSP
  - Bus Interfaces
  - Bridges
  - Processors

- Nios & ARM Processors

- Web-Based IP Deployment
Customization - The Way You Want It

- Table of Active Components
- Configure Each Component
  - Interrupt Request (IRQ)
  - Base Address
  - Hardware Parameters
  - Software Parameters
- Wizard-Based Configuration
Integration

- **Bus Connection**
  - Patch Panel

- **Avalon Switch Fabric**
  - Slave-Side Arbitration
  - Optimized for Throughput

- **Bus Bridging**
  - AMBA™ Advanced High-Performance Bus (AHB)
  - PCI
  - More to Follow . . .
## SOPC Builder Ready Components

<table>
<thead>
<tr>
<th>Component</th>
<th>DMA</th>
<th>USB 1.1</th>
<th>SDRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARM922T Processor</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nios Processor</td>
<td>PCI</td>
<td>USB 2.0</td>
<td>SSRAM</td>
</tr>
<tr>
<td>ARM-to-Nios Bridge (AMBA AHB-to-Avalon)</td>
<td>GPIO</td>
<td>SPI</td>
<td>SRAM</td>
</tr>
<tr>
<td>Interface to User Logic</td>
<td>Timer</td>
<td>CAN 2.0</td>
<td>FLASH</td>
</tr>
<tr>
<td>10/100 Ethernet</td>
<td>Watchdog</td>
<td>16550S UART</td>
<td>On-Chip ROM On-Chip RAM</td>
</tr>
</tbody>
</table>

### 33 IP Cores Now . . .
The List Keeps Growing
# Nios OS / RTOS / Software Support

<table>
<thead>
<tr>
<th>Provider</th>
<th>Product</th>
<th>Description</th>
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<tbody>
<tr>
<td>Accelerated Technology</td>
<td>Nucleus Plus</td>
<td>Royalty-Free, Source-Available RTOS</td>
</tr>
<tr>
<td>Microtronix</td>
<td>µClinux</td>
<td>Open-Source OS</td>
</tr>
<tr>
<td>Micrium</td>
<td>µC/OS-II</td>
<td>Royalty-Free, Preemptive RTOS</td>
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<tr>
<td>MiSPO Co., Ltd.</td>
<td>NORTi</td>
<td>µITRON 4.0-Compatible Real-Time Kernel</td>
</tr>
<tr>
<td>Shugyo Design</td>
<td>KROS</td>
<td>Small-Footprint, Royalty-Free, POSIX-Compliant RTOS</td>
</tr>
<tr>
<td>IAR Systems</td>
<td>visualSTATE</td>
<td>Generates C/C++ Code from Graphical State Machine Model</td>
</tr>
</tbody>
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Nios Development Board, Cyclone Edition
Linux Development Kit

- Open-Source Linux Operating System
  - µCLinux Kernel v2.4.x & Source
  - Embedded Libraries & Source
- SOPC Builder Operating System Component
  - GUI-Based Linux Kernel Configuration
  - Builds Custom a Kernel Based on Nios CPU Configuration in SOPC Builder
- Complete Hardware & Software for Embedded Linux Development
  - µClinux Source Code
  - Daughter Cards for Linux Development
    - OS Support Daughter Board
    - SDRAM/Flash Memory Module
    - Ethernet Development Kit
  - Reference Designs
- Various Linux Kits & Services Available
  - Evaluation Kit Starting at $495
- For Use with Nios Development Kit, APEX Edition (EXCALIBUR-NIOS)

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Thank You!

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