8404121 PROCESSOR DESIGN

Exercise based on the design flow and instruction coding lectures

6. Design an instruction set including addressing modes, and encode the complete set to 16-bit instructions. The desirable features are:
   - Data wordlength 16 bits
   - 16 general-purpose registers
   - Arithmetic flags **C**arry, **N**egative, **Z**ero, o**V**erflow
   - Load/store architecture
   - One 16-bit word / instruction only
   - 1 instruction cycle execution of all instructions

   Dynamic distribution of operations in the algorithms used are:

Operation	%
Data load from memory	30
Multiplication (16x16=32-bit)	15
Addition (16-bit)	13
Addition (32-bit)	9
Subtract (16-bit)	8
Data load from instruction (immediate)	5
Data store	5
Conditional branch	5
Unconditional branch	2
Subroutine call	2
Return from subroutine	2
Shift ± 1-15 bits	2
AND, OR, XOR, INVERT (altogether)	1.6
Multiplication (32x32=64-bit)	0.2
Addition (64-bit)	0.2

   Distribution of shifts, immediate values and branch (and call) offsets or addresses:

Size in bits	Shifts %	Constants %	Branches %
1 bit	40	-	-
2-4 bits	30	40	50
5-8 bits	20	40	30
9-12 bits	5	10	5
13-16 bits	5	10	15

Try to achieve as efficient and usable instruction set/encoding as possible.