8404121 PROCESSOR DESIGN

Excercises based on the design flow and instruction coding lectures

4. Design the most uniform encoding possible for the operations and addressing modes given in the table below. There are 32 registers and data word length is 32 bits. How big is the usable address space for data and instructions, if instruction word length is also 32 bits.

Instruction mnemonic	operands	dest. address	source address	other
ADD dest, src1, src2	3	register	register	
SUB dest, src1, src2	3	register	register	
MPY dest, src1, src2	3	register	register	
LD dest, source	2	register	reg.indirect, immed.	
ST dest, source	2	reg.indirect	register	
SHL dest, source	2	register	register	1-bit shift
SHR dest, source	2	register	register	1-bit shift
BR address	1		reg.indirect, immed.	
BC.cc address	1		immediate	20 conditions
BAL link-reg, address	2	register	immediate	
BALR link-reg, address	2	register	register	

5. Sketch an initial architecture for the data and control parts of a processor implementing this instruction set.